CY284108

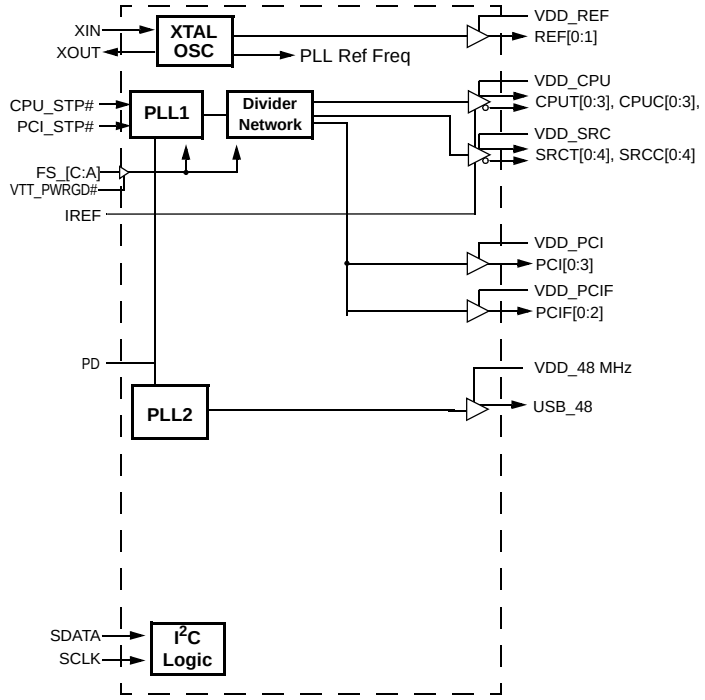
Clock Generator for Intel®Blackford and Bayshore Chipsets

Features

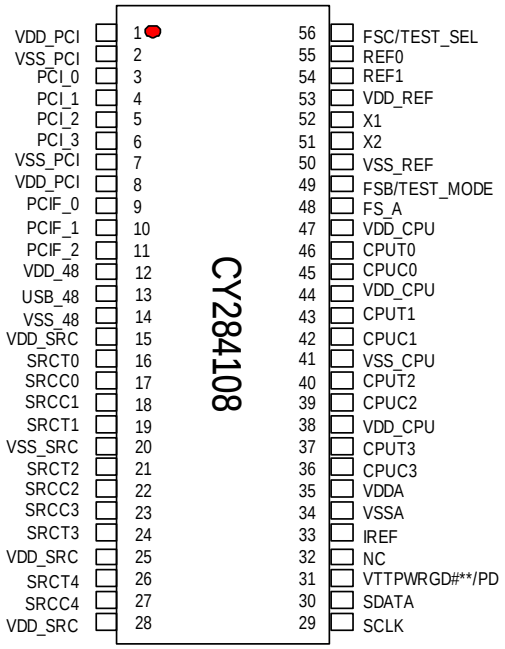
- **Compliant with Intel® CK410B**
- **Supports Intel Pentium-4 and Xeon CPUs**
- **Selectable CPU frequencies**
- **Four differential CPU clock pairs**
- **Five 100 MHz Differential SRC clock pairs**
- **Two buffered Reference Clocks @ 14.31818 MHz**
- **One 48 MHz USB clock**
- **Seven 33 MHz PCI clocks**
- **Low-voltage frequency select input**
- **I²C™ support with readback capabilities**
- **Ideal Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction**
- **3.3V power supply**
- **56-pin SSOP and TSSOP packages**

CPU	SRC	PCI	REF	USB
x 4	x5	x 7	x 2	x 1

Block Diagram



Pin Configuration



400 West Cesar Chavez, Austin, TX 78701 1+(512) 416-8500 1+(512) 416-9669 www.silabs.com

Pin Description

Name	Pin Number	Type	Description
X1	52	I	14.18 MHz crystal input
X2	51	O, SE	14.18 MHz crystal output
REF[1:0]	55, 54	O, SE	14.18 MHz reference clock
PCI[3:0]	6,5,4,3	O, SE	33 MHz clocks
PCIF[2:0]	11,10,9	O,SE	33 MHz free running clock. Is not disabled via Software PCI_STOP.
USB_48	13	O, SE	Fixed 48 MHz USB clock output
CPU[T/C][3:0]	37,36;40,39; 43,42;46,45	O, DIF	Differential CPU clock outputs
SRC[T/C][4:0]	26,27;24,23; 21,22;19,18; 16,17	O, DIF	Differential serial reference clocks. SRC[T/C]4 is recommended for SATA.
FS_A	48	I	3.3V-tolerant input for CPU frequency selection. Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.
FS_B/TEST_MODE	49	I	3.3V-tolerant inputs for CPU frequency selection/selects REF/N or Hi-Z when in test mode. Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications. At VTTPWRGD# asserted low (see page 10 for diagram), this pin is sampled to determine test mode functionality 0 = Hi-Z 1 = REF/N
FS_C/TEST_SEL	56	I	3.3V-tolerant inputs for CPU frequency selection/selects test mode if pulled to 3.3V when VTT_PWRGD# is asserted low (seepage 10 for diagram). Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications
IREF	33	I	A precision resistor is attached to this pin, which is connected to the internal current reference
VTT_PWRGD#/PD	31	I, PD	DF3.3V LVTTL input is a level sensitive strobe used to latch the FS_A, FS_B, FS_C/TEST_SEL inputs. After VTT_PWRGD# (active low) assertion, this pin becomes a realtime input for asserting power down (active high). See page 10 for diagram.
SCLK	29	I	SMBus-compatible SCLOCK
SDATA	30	I/O	SMBus-compatible SDATA
VDD_REF	53	PWR	3.3V power supply for outputs
VSS_REF	50	GND	Ground for outputs
VDD_PCI	1,8	PWR	3.3V power supply for outputs
VSS_PCI	2,7	GND	Ground for outputs
VDD_48	12	PWR	3.3V power supply for outputs
VSS_48	14	GND	Differential CPU clock outputs
VDD_SRC	15,25,28	PWR	3.3V power supply for outputs
VSS_SRC	20	GND	Ground for outputs
VDD_CPU	38,44,47	PWR	3.3V power supply for outputs
VSS_CPU	41	GND	Ground for outputs
VDD_A	35	PWR	3.3V power supply for outputs
VSS_A	34	GND	Ground for outputs
NC	32	–	No Connection

Table 1. CPU Frequency Select Tables

FS_C	FS_B	FS_A	CPU	SRC	PCIF/PCI	REF0	DOT96	USB
MID	0	1	100 MHz	100 MHz	33 MHz	14.318 MHz	96 MHz	48 MHz
0	0	1	133 MHz	100 MHz	33 MHz	14.318 MHz	96 MHz	48 MHz
0	1	1	166MHz	100MHz	33MHz	14.318MHz	96MHz	48MHz
0	1	0	200MHz	100MHz	33MHz	14.318MHz	96MHz	48MHz
0	0	0	266MHz	100MHz	33MHz	14.318MHz	96MHz	48MHz
MID	0	0	333MHz	100MHz	33MHz	14.318MHz	96MHz	48MHz
MID	1	0	400MHz	100MHz	33MHz	14.318MHz	96MHz	48MHz
MID	1	1	Reserved	100MHz	33MHz	14.318MHz	96MHz	48MHz
1	0	x	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	1	0	REF/2	REF/8	REF/24	REF	REF	REF
1	1	1	REF/2	REF/8	REF/24	REF	REF	REF

Frequency Select Pins (FS_[C:A])

Host clock frequency selection is achieved by applying the appropriate logic levels to FS_A, FS_B, FS_C inputs prior to VTT_PWRGD# assertion (as seen by the clock synthesizer). Upon VTT_PWRGD# being sampled low by the clock chip (indicating processor VTT voltage is stable), the clock chip samples the FS_A, FS_B, and FS_C input values. For all logic levels of FS_A, FS_B, and FS_C, VTT_PWRGD# employs a one-shot functionality in that once a valid low on VTT_PWRGD# has been sampled, all further VTT_PWRGD#, FS_A, FS_B, and FS_C transitions will be ignored, except in test mode. FS_C is a three level input, when sampled at a voltage greater than 2.0V by VTTPWRGD#, the device will enter test mode as selected by the voltage level on the FS_B input.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 2*.

The block write and block read protocol is outlined in *Table 3* while *Table 4* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 2. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

Table 3. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address – 7 bits	8:2	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code – 8 bits	18:11	Command Code – 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count – 8 bits (Skip this step if I^2C_EN bit set)	20	Repeat start
28	Acknowledge from slave	27:21	Slave address – 7 bits
36:29	Data byte 1 – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2 – 8 bits	37:30	Byte Count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave – 8 bits
....	Data Byte N –8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave – 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave / Acknowledge
		....	Data Byte N from slave – 8 bits
		....	NOT Acknowledge
		....	Stop

Table 4. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address – 7 bits	8:2	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code – 8 bits	18:11	Command Code – 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte – 8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address – 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave – 8 bits
		38	NOT Acknowledge
		39	Stop

Control Registers

Byte 0: Control Register 0

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	1	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	1	SRC[T/C]4	SRC[T/C]4 Output Enable 0 = Disable (Tri-state), 1 = Enable
3	1	SRC[T/C]3	SRC[T/C]3 Output Enable 0 = Disable (Tri-state), 1 = Enable
2	1	SRC[T/C]2	SRC[T/C]2 Output Enable 0 = Disable (Tri-state), 1 = Enable
1	1	SRC[T/C]1	SRC[T/C]1 Output Enable 0 = Disable (Tri-state), 1 = Enable
0	1	SRC[T/C]0	SRC[T/C]0 Output Enable 0 = Disable (Tri-state), 1 = Enable

Byte 1: Control Register 1

Bit	@Pup	Name	Description
7	1	REF1	REF1 Output Enable 0 = Disable, 1 = Enable
6	1	REF0	REF0 Output Enable 0 = Disable, 1 = Enable
5	1	CPU[T/C]3	CPU[T/C]3 Output Enable 0 = Disable (Tri-state), 1 = Enable
4	1	CPU[T/C]2	CPU[T/C]2 Output Enable 0 = Disable (Tri-state), 1 = Enable
3	1	RESERVED	RESERVED
2	1	CPU[T/C]1	CPU[T/C]1 Output Enable 0 = Disable (Tri-state), 1 = Enable
1	1	CPU[T/C]0	CPU[T/C]0 Output Enable 0 = Disable (Tri-state), 1 = Enable
0	0	CPU SRC PCIF PCI	PLL1 Spread Spectrum Enable 0 = Spread off, 1 = Spread on

Byte 2: Control Register 2

Bit	@Pup	Name	Description
7	1	PCI3	PCI3 Output Enable 0 = Disable, 1 = Enable
6	1	PCI2	PCI2 Output Enable 0 = Disable, 1 = Enable
5	1	PCI1	PCI1 Output Enable 0 = Disable, 1 = Enable
4	1	PCI0	PCI0 Output Enable 0 = Disable, 1 = Enable
3	1	PCIF2	PCIF2 Output Enable 0 = Disable, 1 = Enable
2	1	PCIF1	PCIF1 Output Enable 0 = Disable, 1 = Enable
1	1	PCIF0	PCIF0 Output Enable 0 = Disable, 1 = Enable

Byte 2: Control Register 2 (continued)

Bit	@Pup	Name	Description
0	1	USB48	USB_48 Output Enable 0 = Disable, 1 = Enable

Byte 3: Control Register 3

Bit	@Pup	Name	Description
7	0	PCIF2	Allow control of PCIF2 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with SW PCI_STP#
6	0	PCIF1	Allow control of PCIF1 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with SW PCI_STP#
5	0	PCIF0	Allow control of PCIF0 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with SW PCI_STP#
4	0	SRC[T/C]4	Allow control of SRC[T/C]4 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
3	0	SRC[T/C]3	Allow control of SRC[T/C]3 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
2	0	SRC[T/C]2	Allow control of SRC[T/C]2 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
1	0	SRC[T/C]1	Allow control of SRC[T/C]1 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
0	0	SRC[T/C]0	Allow control of SRC[T/C]0 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#

Byte 4: Control Register 4

Bit	@Pup	Name	Description
7	0	CPU[T/C]3	CPU[T/C]3 PD drive mode 0 = Driven in power down, 1 = Tri-state
6	0	CPU[T/C]2	CPU[T/C]2 PD drive mode 0 = Driven in power down, 1 = Tri-state
5	0	CPU[T/C]1	CPU[T/C]1 PD drive mode 0 = Driven in power down, 1 = Tri-state
4	0	CPU[T/C]0	CPU[T/C]0 PD drive mode 0 = Driven in power down, 1 = Tri-state
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

Byte 5: Control Register 5

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	SRC[T/C][4:0] PCI_STP# drive mode	Stoppable SRC[T/C][4:0] drive mode upon PCI_STP# assertion 0 = Driven in PCI_STOP#, 1 = Tri-state
5	0	SRC[T/C][4:0] PWRDWN Drive mode	SRC[T/C][4:0] PWRDWN drive mode 0 = Driven in power down, 1 = Tri-state
4	0	RESERVED	RESERVED, Set = 0
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED

Byte 5: Control Register 5 (continued)

Bit	@Pup	Name	Description
0	0	RESERVED	RESERVED

Byte 6: Control Register 6

Bit	@Pup	Name	Description
7	0	TEST_SEL	REF/N or Tri-state Select 0 = Tri-state, 1 = REF/N Clock
6	0	TEST_MODE	Test Clock Mode Entry Control 0 = Normal operation, 1 = REF/N or Tri-state mode
5	0	RESERVED	RESERVED, Set = 0
4	1	REF	REF Output Drive Strength 0 = Low, 1 = High
3	1	PCI_Stop Control	SW PCI_STP# Function 0 = SW PCI_STP# assert, 1 = SW PCI_STP# deassert When this bit is set to 0, all STOPPABLE PCI, PCIF and SRC outputs will be stopped in a synchronous manner with no short pulses. When this bit is set to 1, all STOPPED PCI, PCIF and SRC outputs will resume in a synchronous manner with no short pulses.
2	HW	FS_C	FS_C Reflects the value of the FS_C pin sampled on power up 0 = FS_C was low during VTT_PWRGD# assertion
1	HW	FS_B	FS_B Reflects the value of the FS_B pin sampled on power up 0 = FS_B was low during VTT_PWRGD# assertion
0	HW	FS_A	FS_A Reflects the value of the FS_A pin sampled on power up 0 = FS_A was low during VTT_PWRGD# assertion

Byte 7: Vendor ID

Bit	@Pup	Name	Description
7	0	Revision Code Bit 3	Revision Code Bit 3
6	0	Revision Code Bit 2	Revision Code Bit 2
5	0	Revision Code Bit 1	Revision Code Bit 1
4	0	Revision Code Bit 0	Revision Code Bit 0
3	1	Vendor ID Bit 3	Vendor ID Bit 3
2	0	Vendor ID Bit 2	Vendor ID Bit 2
1	0	Vendor ID Bit 1	Vendor ID Bit 1
0	0	Vendor ID Bit 0	Vendor ID Bit 0

Table 5. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Tolerance (max.)	Stability (max.)	Aging (max.)
14.31818 MHz	AT	Parallel	20 pF	0.1 mW	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

The CY284108 requires a parallel resonance crystal. Substituting a series resonance crystal will cause the CY284108 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL).

Figure shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. It is a common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal. This is not true.

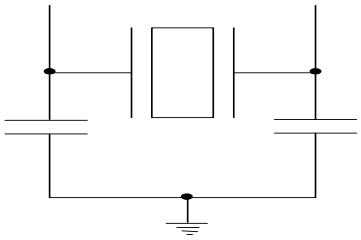


Figure 1. Crystal Capacitive Clarification

Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.

Figure 2.

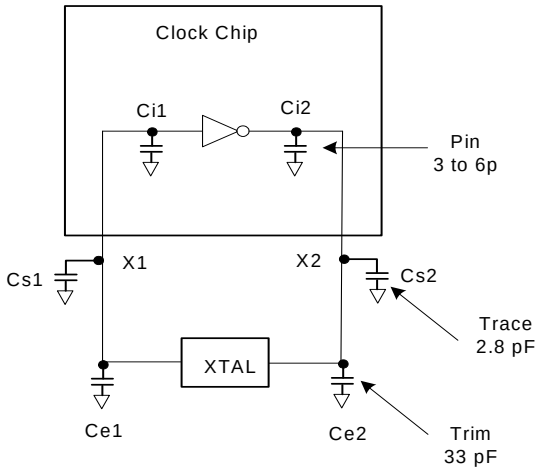


Figure 3. Crystal Loading Example

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$Ce = 2 * CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

CL.....Crystal load capacitance

CLe..... Actual loading seen by crystal using standard value trim capacitors

Ce..... External trim capacitors

Cs.....Stray capacitance (terraced)

Ci .....Internal capacitance (lead frame, bond wires etc.)

PD (Power-down) Clarification

The VTT_PWRGD# /PD pin is a dual-function pin. During initial power up, the pin functions as VTT_PWRGD#. Once VTT_PWRGD# has been sampled low by the clock chip, the pin assumes PD functionality. The PD pin is an asynchronous active HIGH input used to shut off all clocks cleanly prior to shutting off power to the device. This signal is synchronized internal to the device prior to powering down the clock synthesizer. PD is also an asynchronous input for powering up the system. When PD is asserted high, drive all clocks to a low value and hold prior to turning off the VCOs and the crystal oscillator.

PD (Power-down) Assertion

When PD is sampled high by two consecutive rising edges of CPUC, all single-ended outputs will be held low on their next high to low transition and differential clocks must held high or tri-stated (depending on the state of the control register drive mode bit) on the next diff clock# high to low transition within 4 clock periods. When the SMBus PD drive mode bit corresponding to the differential (CPU and SRC) clock output of interest is programmed to '0', the clock outputs are held with "Diff clock" pin driven high at 2 x Iref, and "Diff clock#" tri-state. If the control register PD drive mode bit corresponding to the output of interest is programmed to "1", then both the "Diff clock" and the "Diff clock#" are tri-state. Note that *Figure 4* shows CPUT = 133 MHz and PD drive mode = '1' for all differential outputs. This diagram and description is applicable to valid CPU frequencies 100, 133, 166, 200, 266, 333, and 400 MHz. In the event that PD mode is desired as the initial power-on state, PD must be asserted high in less than 10 μs after asserting Vtt_PwrGd#.

PD Deassertion

The power-up latency is less than 1.8 ms. This is the time from the deassertion of the PD pin or the ramping of the power supply until the time that stable clocks are output from the clock chip. All differential outputs stopped in a three-state condition resulting from power down will be driven high in less than 300 μs of PD deassertion to a voltage greater than 200 mV. After the clock chip's internal PLL is powered up and locked, all outputs will be enabled within a few clock cycles of each other. *Figure 5* is an example showing the relationship of clocks coming up.

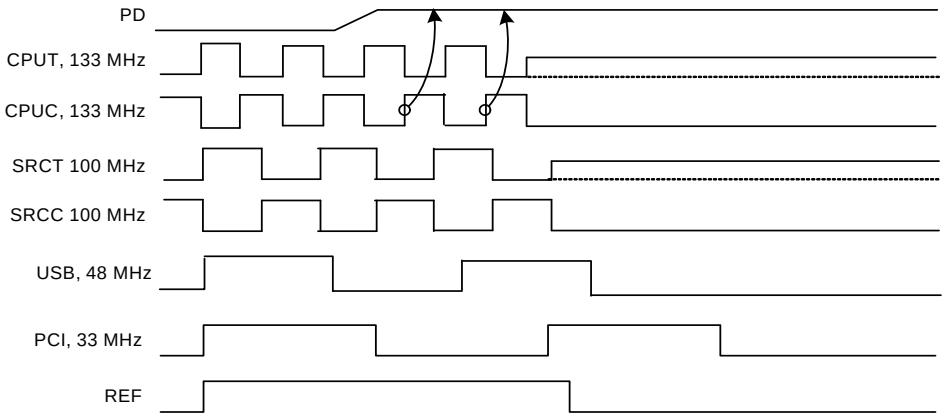


Figure 4. Power-down Assertion Timing Waveform

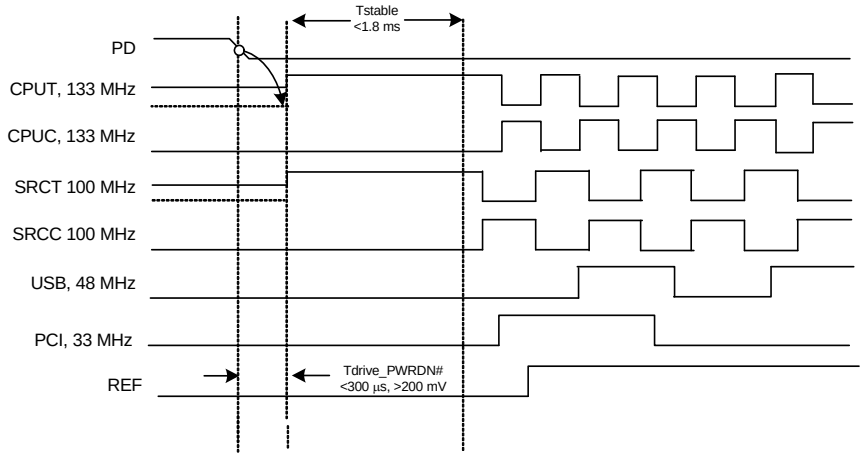


Figure 5. Power-down Deassertion Timing Waveform

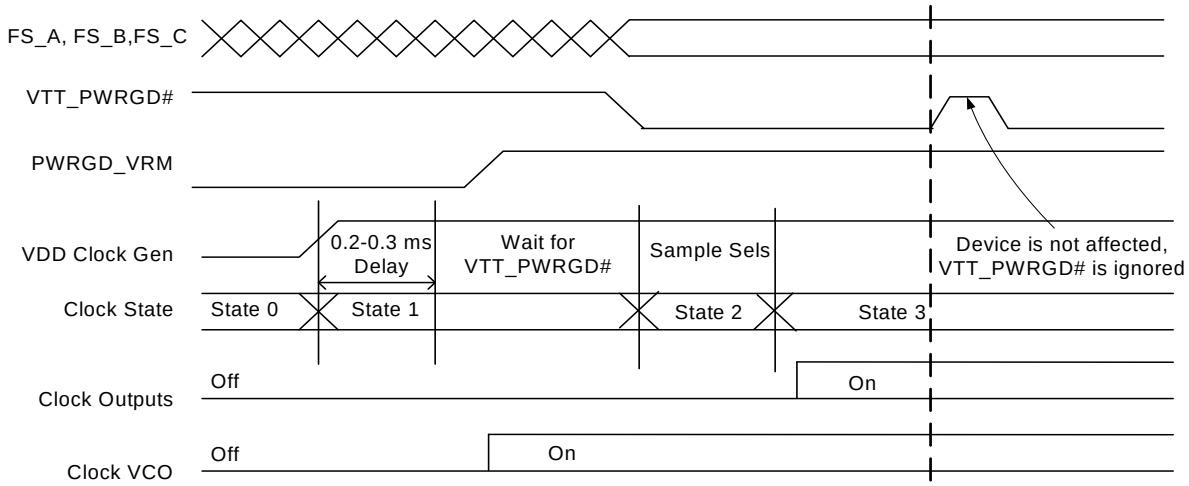


Figure 6. VTT_PWRGD# Timing Diagram

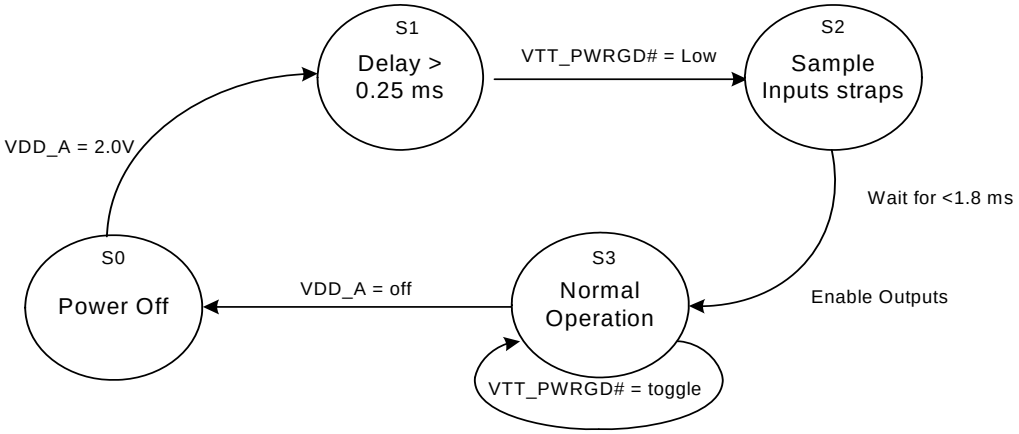


Figure 7. Clock Generator Power-up/Run State Diagram

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	Core Supply Voltage		–0.5	4.6	V
V_{DD_A}	Analog Supply Voltage		–0.5	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non-functional	–65	150	°C
T_A	Temperature, Operating Ambient	Functional	0	70	°C
T_J	Temperature, Junction	Functional	–	150	°C
$Ø_{JC}$	Dissipation, Junction to Case	Mil-STD-883E Method 1012.1	–	20	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	–	60	°C/W
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V
UL-94	Flammability Rating	At 1/8 in.	V–0		
MSL	Moisture Sensitivity Level		1		

Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
All VDDs	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V_{ILI2C}	Input Low Voltage	SDATA, SCLK	–	1.0	V
V_{IHI2C}	Input High Voltage	SDATA, SCLK	2.2	–	V
V_{IL_FS}	FS_[A:B] Input Low Voltage		V_{SS} – 0.3	0.35	V
V_{IH_FS}	FS_[A:B] Input High Voltage		0.7	V_{DD} + 0.5	V
V_{IMFS_C}	FS_C Mid Range		0.7	2.0	V
$V_{IH\ FS_C}$	FS_C High Range		2.0	V_{DD} + 0.3	V
V_{IL}	3.3V Input Low Voltage		V_{SS} – 0.3	0.8	V
V_{IH}	3.3V Input High Voltage		2.0	V_{DD} + 0.3	V
I_{IL}	Input Low Leakage Current	Except internal pull-up resistors, $0 < V_{IN} < V_{DD}$	–5	–	µA
I_{IH}	Input High Leakage Current	Except internal pull-down resistors, $0 < V_{IN} < V_{DD}$	–	5	µA
V_{OL}	3.3V Output Low Voltage	I_{OL} = 1 mA	–	0.4	V
V_{OH}	3.3V Output High Voltage	I_{OH} = –1 mA	2.4	–	V
I_{OZ}	High-impedance Output Current		–10	10	µA
C_{IN}	Input Pin Capacitance		3	5	pF
C_{OUT}	Output Pin Capacitance		3	6	pF
L_{IN}	Pin Inductance		–	7	nH
V_{XIH}	Xin High Voltage		$0.7V_{DD}$	V_{DD}	V
V_{XIL}	Xin Low Voltage		0	$0.3V_{DD}$	V
$I_{DD3.3V}$	Dynamic Supply Current	At max. load and freq. per *Figure 9*	–	500	mA
$I_{PD3.3V}$	Power-down Supply Current	PD asserted, Outputs Driven	–	70	mA
$I_{PT3.3V}$	Power-down Supply Current	PD asserted, Outputs Tri-state	–	12	mA

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					
T_{DC}	XIN Duty Cycle	The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification	47.5	52.5	%
T_{PERIOD}	XIN Period	When XIN is driven from an external clock source	69.841	71.0	ns
T_R / T_F	XIN Rise and Fall Times	Measured between $0.3V_{DD}$ and $0.7V_{DD}$	–	10.0	ns
T_{CCJ}	XIN Cycle to Cycle Jitter	As an average over 1-μs duration	–	500	ps
L_{ACC}	Long-term Accuracy	Over 150 ms	–	300	ppm
CPU at 0.7V					
T_{DC}	CPUT and CPUC Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	100-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	9.997001	10.00300	ns
T_{PERIOD}	133-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	7.497751	7.502251	ns
T_{PERIOD}	166-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	5.998201	6.001801	ns
T_{PERIOD}	200-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	4.998500	5.001500	ns
T_{PERIOD}	266-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	3.748875	3.751125	ns
T_{PERIOD}	333-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	2.999100	3.000900	ns
T_{PERIOD}	400-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	2.499250	2.500750	ns
T_{SKEW}	CPU0 to CPU1	Measured at crossing point V_{OX}	–	100	ps
T_{CCJ}	CPUT/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	85	ps
L_{ACC}	Long Term Accuracy	Measured using frequency counter over 0.15seconds.	–	300	ppm
T_R / T_F	CPUT and CPUC Rise and Fall Times	Measured from V_{OL} = 0.175 to V_{OH} = 0.525V	175	1100	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2 * (T_R - T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise Time Variation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps
V_{HIGH}	Voltage High	Math averages *Figure 9*	660	850	mV
V_{LOW}	Voltage Low	Math averages *Figure 9*	–150	–	mV
V_{OX}	Crossing Point Voltage at 0.7V Swing		250	550	mV
V_{OVS}	Maximum Overshoot Voltage		–	V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V_{RB}	Ring Back Voltage	See *Figure 9*. Measure SE	–	0.2	V
SRC					
T_{DC}	SRCT and SRCC Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	100-MHz SRCT and SRCC Period	Measured at crossing point V_{OX}	9.997001	10.00300	ns
T_{SKEW}	Any SRCT/C to SRCT/C Clock Skew	Measured at crossing point V_{OX}	–	250	ps
T_{CCJ}	SRCT/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	125	ps
L_{ACC}	SRCT/C Long Term Accuracy	Measured at crossing point V_{OX}	–	300	ppm
T_R / T_F	SRCT and SRCC Rise and Fall Times	Measured from V_{OL} = 0.175 to V_{OH} = 0.525V	175	1100	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2 * (T_R - T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise TimeVariation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps
V_{HIGH}	Voltage High	Math averages *Figure 9*	660	850	mV

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
V_{LOW}	Voltage Low	Math averages *Figure 9*	–150	–	mV
V_{OX}	Crossing Point Voltage at 0.7V Swing		210	550	mV
V_{OVS}	Maximum Overshoot Voltage		–	V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V_{RB}	Ring Back Voltage	See *Figure 9.* Measure SE	–	0.2	V
PCI/PCIF					
T_{DC}	PCI Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	29.99100	30.00900	ns
$T_{PERIODSS}$	Spread Enabled PCIF/PCI Period, SSC	Measurement at 1.5V	29.9910	30.15980	ns
T_{HIGH}	PCIF and PCI High Time	Measurement at 2.4V	12.0	–	ns
T_{LOW}	PCIF and PCI Low Time	Measurement at 0.4V	12.0	–	ns
T_R / T_F	PCI Edge Rates	Measured between 0.8V and 2.0V	0.89	4.0	V/ns
T_{SKEW}	Any PCI Clock to Any PCI clock Skew	Measurement at 1.5V	–	585	ps
T_{CCJ}	PCIF and PCI Cycle to Cycle Jitter	Measurement at 1.5V	–	500	ps
USB48					
T_{DC}	USB Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	USB Period,	Measurement at 1.5V, mean value over 1 μs	20.8271	20.8396	ns
L_{ACC}	Long Accuracy	Measured at 1.5V using frequency counter over 0.15s	–	100	ppm
T_{HIGH}	USB High Time	Measurement at 2.0V	8.094	11.000	ns
T_{LOW}	USB Low Time	Measurement at 0.8V	7.694	11.000	ns
T_R / T_F	USB Edge Rates	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement taken @1.5V waveform	–	350	ps
T_{LTJ}	Long Term Jitter	Measurement taken from cross point V_{OX} @ 1 μs	–	650	ps
TLTJ	Long Term Jitter	Measurement taken from cross point V_{OX} @ 10 μs	–	1	ns
TLTJ	Long Term Jitter	Measurement taken from cross point V_{OX} @ 125 μs	–	1	ns
REF					
T_{DC}	REF Duty Cycle	Measurement at 1.5V	45	55	ns
T_{PERIOD}	REF Period	Measurement at 1.5V	69.827	69.855	ns
T_R / T_F	REF Edge Rates	Measured between 0.8V and 2.0V	0.55	4.0	V/ns
T_{CCJ}	REF Cycle to Cycle Jitter	Measurement at 1.5V	–	1000	ps
T_{SKEW}	REF Clock to Other REF Clock skew	Measurement at 1.5V	–	500	ps
ENABLE/DISABLE and SET-UP					
T_{STABLE}	Clock Stabilization from Power-up		–	1.8	ms

Test and Measurement Set-up

For PCI Single-ended Signals and Reference

Figure 8 shows the test load configurations for the single-ended PCI, USB, and REF output signals.

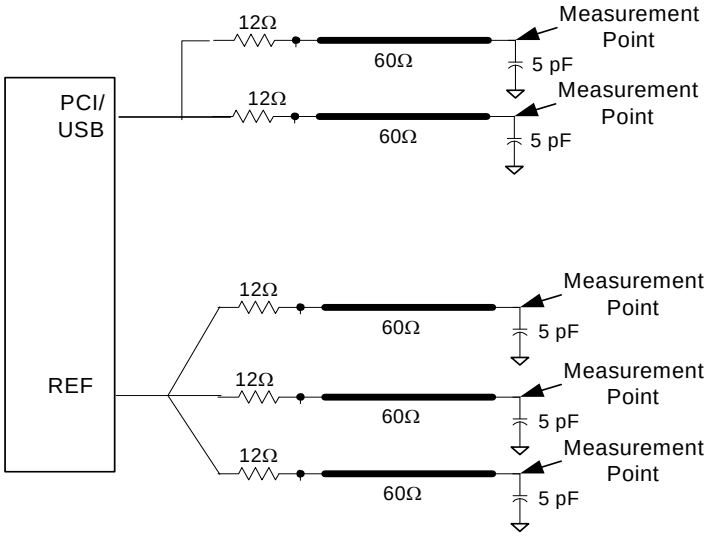


Figure 8. Single-ended Load Configuration

For Differential CPU, SRC and DOT96 Output Signals

Figure 9 shows the test load configuration for the differential CPU and SRC outputs.

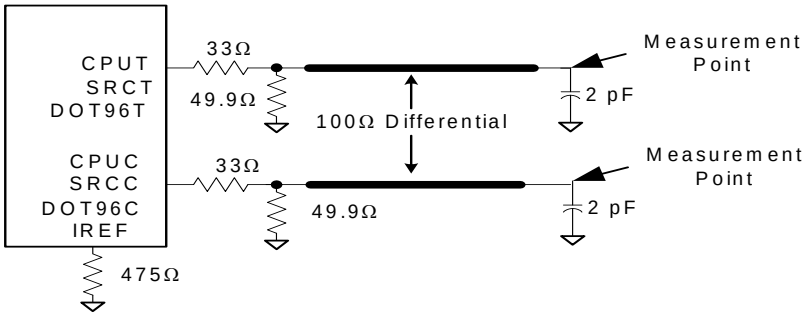


Figure 9. 0.7V Single-ended Load Configuration

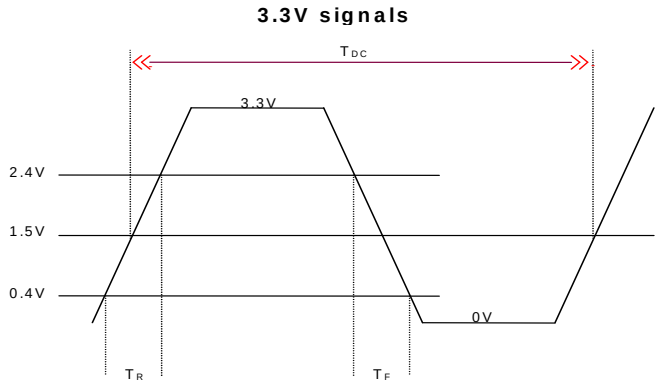


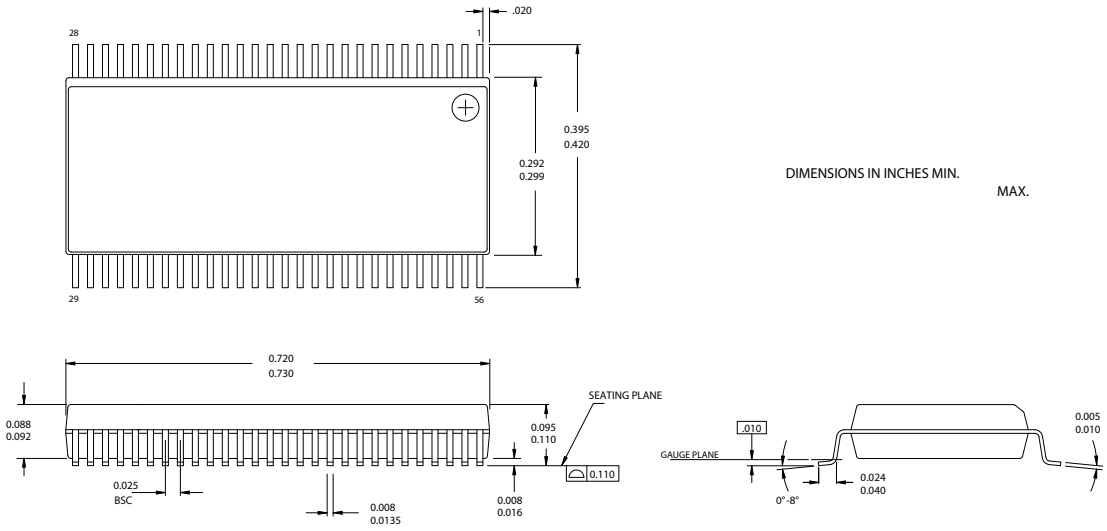
Figure 10. Single-ended Output Signals (for AC Parameters Measurement)

Ordering Information

Part Number	Package Type	Product Flow
Lead-free		
CY284108OXC	56-pin SSOP	Commercial, 0° to 85°C
CY284108OXCT	56-pin SSOP – Tape and Reel	Commercial, 0° to 85°C
CY284108ZXC	56-pin TSSOP	Commercial, 0° to 85°C
CY284108ZXCT	56-pin TSSOP – Tape and Reel	Commercial, 0° to 85°C

Package Diagrams

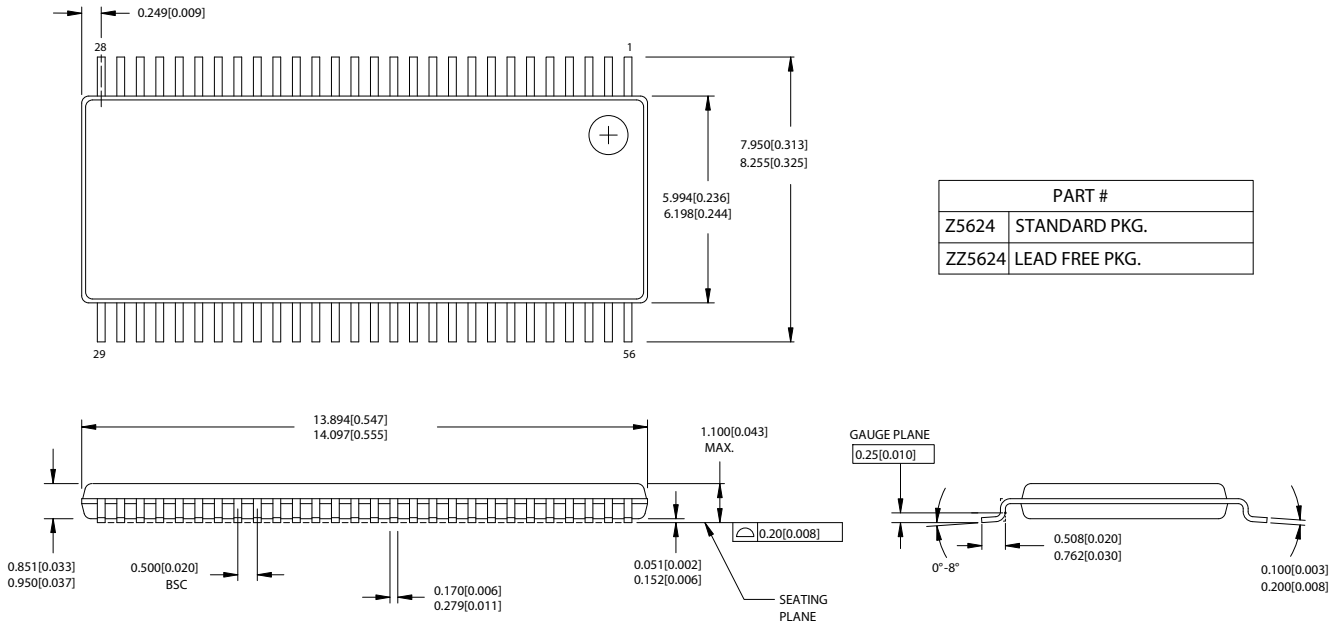
56-Lead Shrunk Small Outline Package O56



Package Diagrams (continued)

56-Lead Thin Shrunk Small Outline Package, Type II (6 mm x 12 mm) Z5624

NOTE :
1. JEDEC STD REF MO-153
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.006 in (0.152 mm) PER SIDE
3. DIMENSIONS IN MM. [INCHES] MIN.
   MAX.
3. PACKAGE WEIGHT 0.42gms



PART #	
Z5624	STANDARD PKG.
ZZ5624	LEAD FREE PKG.

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